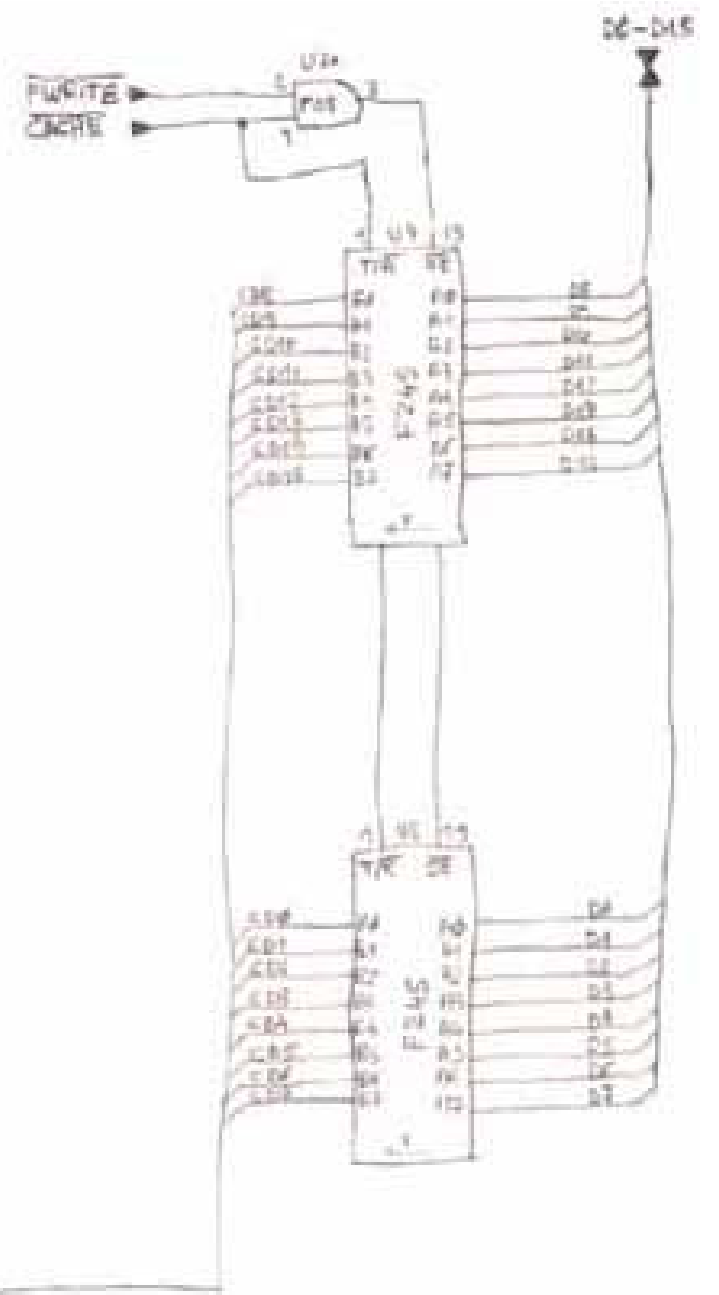


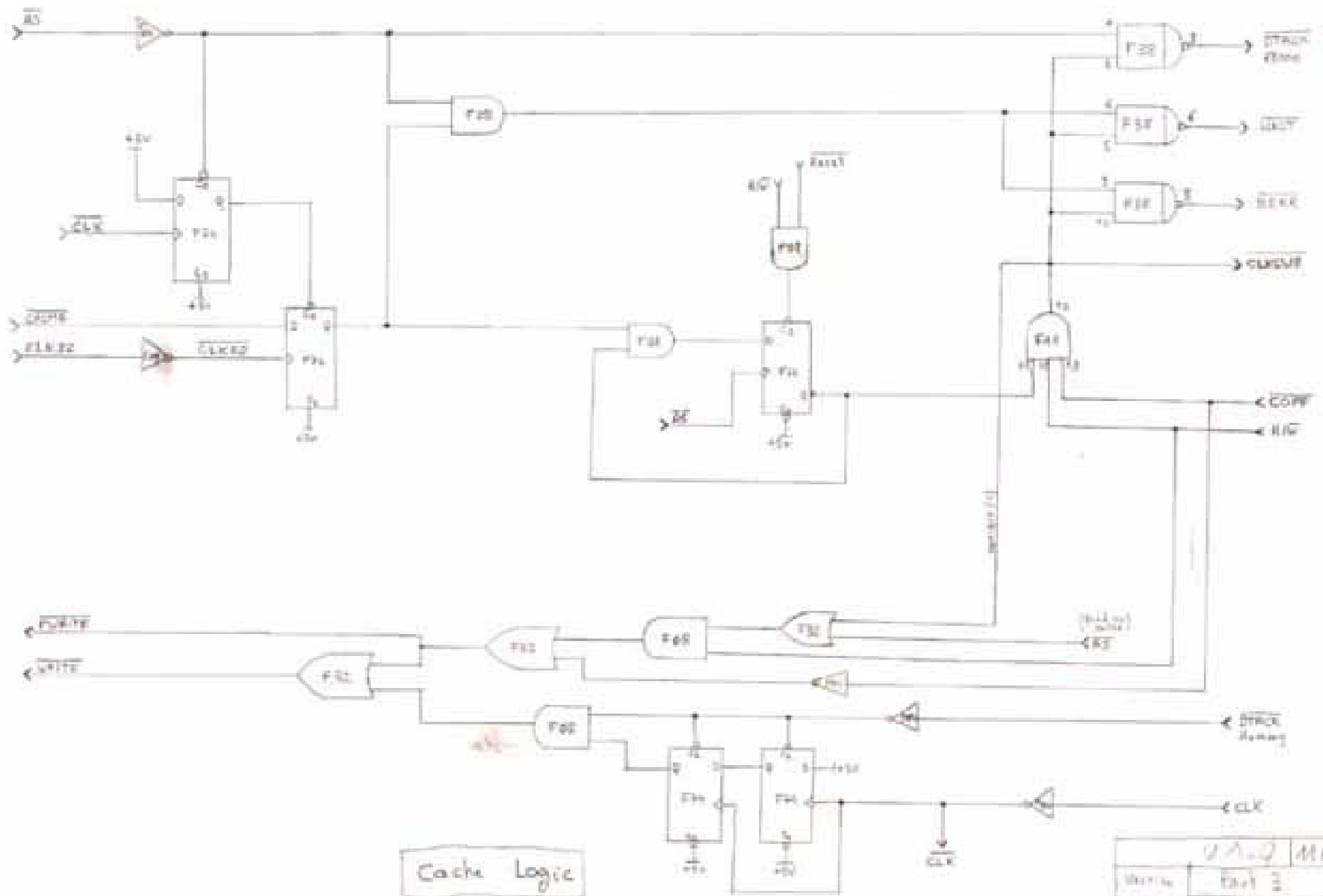
$$T = A \rightarrow B$$

$$\bar{R} = \bar{B} \rightarrow A$$



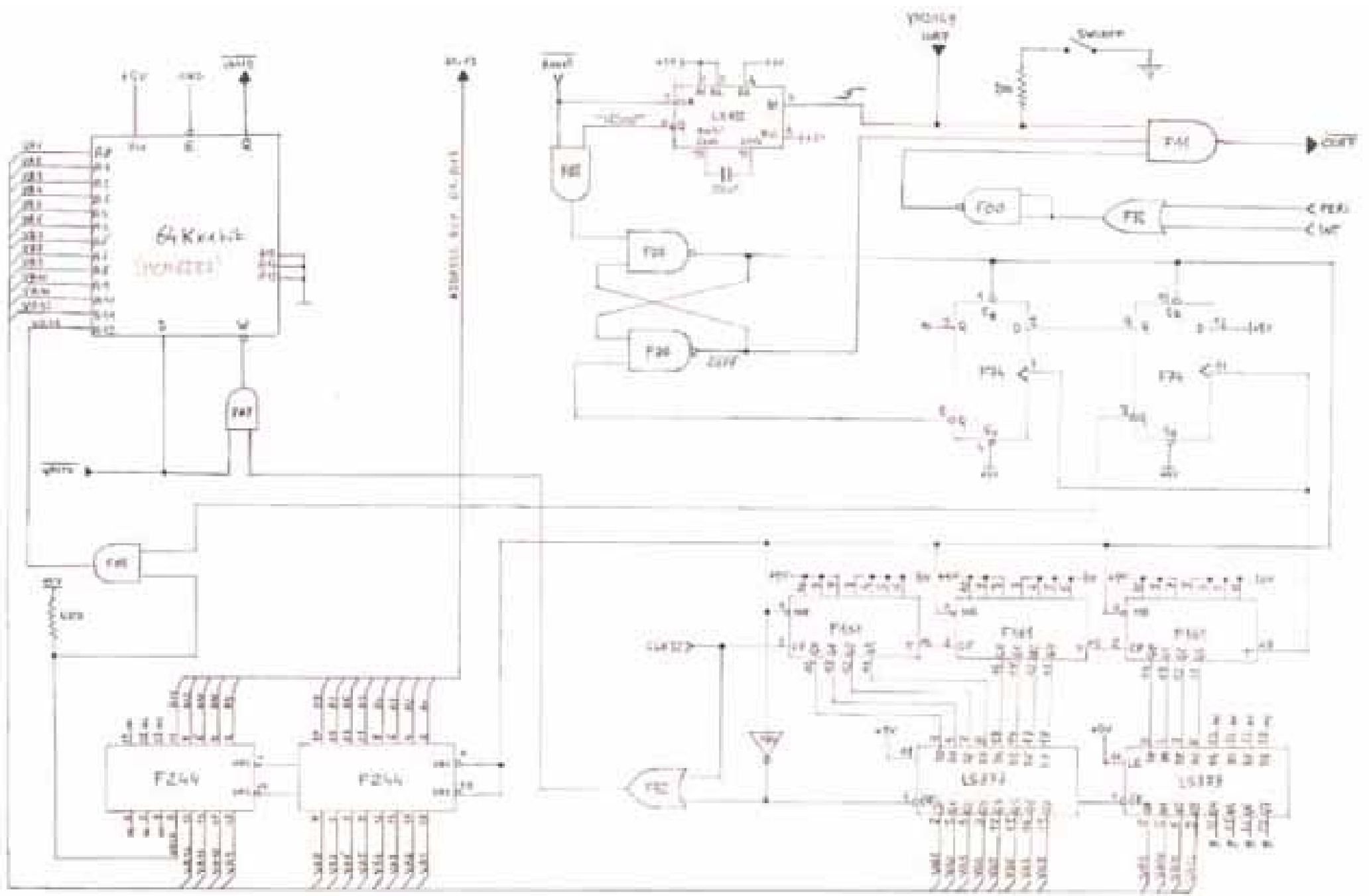
Data RAMS

File # 10-11-12
V.A.O
Part 1
System Cache



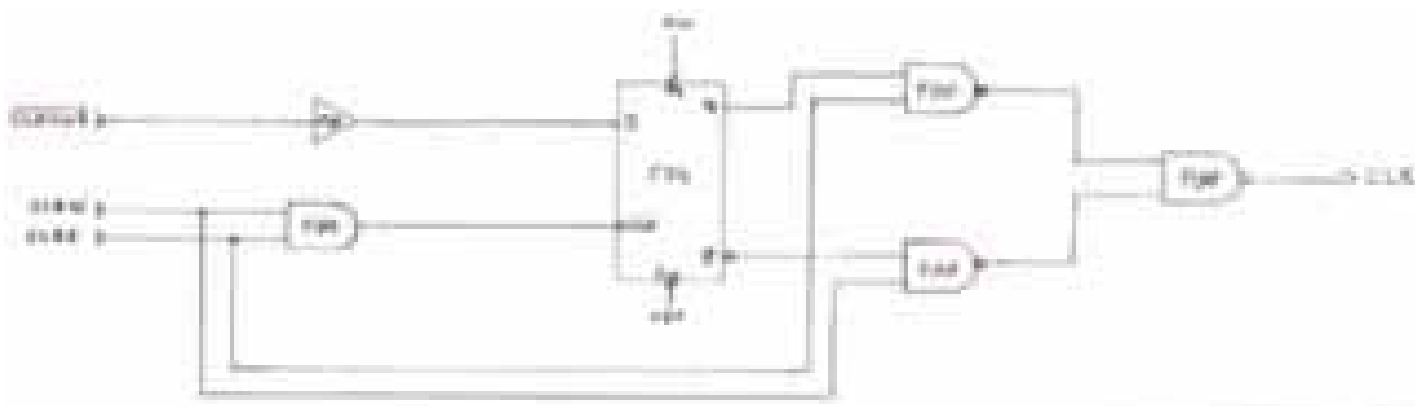
Cache Logic

U.A. 2	M/83
Part 2	
Cache	Cache



Cache Valid Logic

V. 1.0	4/12
Version	Part 4
Author	Centura Cache



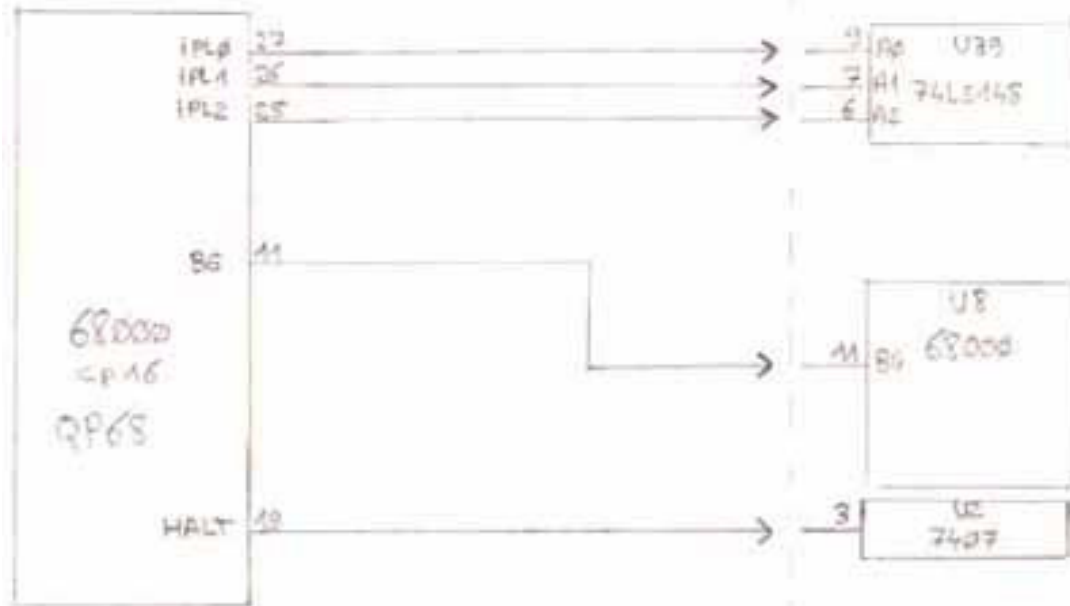
2-bit full adder logic

	V.A.3 4/1/23
Page No.	Page 5
Date	Continue Code

Card

ST

9 solders



Extra BUS Connection

V 1.0 11/89	
Version 16k+ ROMS	Part 6
Centaur Cache	